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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,892	11/21/2003	Dharmesh Jawarani	SC13038TP	1654

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,892	JAWARANI ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-14,17-22,25,26,28,30,31,34-36,44 and 45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,10-14,17-22,25,26,28,30,31,34-36,44 and 45* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/26/2006 has been entered.

Claim Objections

Claim 25 is objected to because of the following informalities: In line 1 of claim 25, "particles" should be changed to "germanium." Appropriate correction is required.

Claim 34 is objected to because of the following informalities: In line 7, "using the gate" should be deleted (this phrase is recited twice). Appropriate correction is required.

Claim 36 is objected to because of the following informalities: In line 8, "a" should be deleted between "implanting" and "boron." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7, 17-22, 26, 28, 30, 31, 36, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. 6,399,452) in view of Koizumi et al. (U.S. 5,475,244).

Regarding claim 1, Krishnan et al. teaches a method of forming a contact to a source/drain contact region of a transistor device having a gate, and the source/drain contact region is comprised substantially of silicon, the method comprising:

- implanting germanium into a region of the source/drain contact region at a dose between 1E13 and 1E17 atoms per centimeter squared using the gate as a mask (region 307 in Fig. 3F; column 3, lines 13-16);
- activating the germanium implanted into the source/drain contact region (column 3, lines 27-32);
- implanting boron into the source/drain contact (column 3, lines 18-21); and
- forming a nickel silicide over the source/drain contact region after the activating to form the contact (column 3, lines 39-43).

Krishnan et al. does not teach that the implanting the boron is performed subsequent to the activating the germanium.

Koizumi et al. teaches a method of forming a transistor that comprises implanting germanium into a source/drain region, activating the germanium implant, and subsequently doping the source/drain region. The method taught by Koizumi et al. ensures a good SiGe mixed crystal (column 11, lines 33-50).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Krishnan et al., and reverse the

order of the germanium activation and dopant implant, as taught by Koizumi et al., since this method yields a good SiGe mixed crystal.

Regarding claim 2, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches that activating the germanium includes making the germanium substitutional in a lattice of the source/drain contact region, wherein the lattice includes silicon (column 3, lines 25-30—the anneal recrystallizes the silicon containing germanium, so the germanium becomes part of the crystal lattice).

Regarding claim 3, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Since Krishnan et al. teaches that the activation processes recrystallizes the germanium-doped silicon (forming a mixed crystal), it is inherent that this process increases the lattice constant in the source/drain contact region, since SiGe has a higher lattice constant than Si (Ge is a larger atom).

Regarding claim 7, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches that the activating includes heating the source/drain contact region to a temperature of greater than 550 C (column 3, lines 36-38).

Regarding claim 17, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches forming a sidewall spacer (305 in Fig. 3E) adjacent to a sidewall of the gate, wherein the implanting the germanium is performed prior to the forming the sidewall spacer (germanium implantation occurs before and after the sidewall spacer is formed—column 2, lines 60-66 and column 3, lines 13-16).

Regarding claim 18, Krishnan et al. and Koizumi et al. together teach the method of claim 17. Krishnan et al. further teaches that forming the sidewall spacer is performed prior to the implanting the source/drain dopant (source/drain dopants are implanted both before and after the sidewall spacer is formed—column 2, line 66 – column 3, line 4 and column 3, lines 15-24).

Regarding claim 19, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches that the gate is over a semiconductor substrate, the source/drain contact region is in the semiconductor substrate, and the source/drain contact region is disposed laterally from the gate (Figs. 3A-3G).

Regarding claim 20, Krishnan et al. and Koizumi et al. together teach the method of claim 19. Krishnan et al. further teaches implanting a second source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant (Krishnan et al. teaches performing two source/drain dopants resulting in regions 305 and 308 respectively in Figs. 3D-3G; the second implantation region, 308, is deeper than the first).

Regarding claims 21 and 22, Krishnan et al. and Koizumi et al. together teach the method of claim 19. Krishnan et al. further teaches implanting the germanium with an energy of at least 3keV and in the range of 3keV to 50 keV (40 keV—column 3, line15).

Regarding claim 25, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches that:

- the transistor has a second source/drain contact;

- the implanting of the further includes implanting the germanium into the second source/drain contact region at the dose between 1E13 and 1E17 atoms per centimeter squared;
- the activating the germanium further includes activating the germanium implanted into the second source/drain contact region; and
- the implanting boron further includes implanting the boron into the second source/drain contact region; further comprising forming a second nickel silicide region to form a second contact (Figs. 3A-3H; column 2, line 60 – column 3, line 43).

Regarding claim 28, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches that the gate is over a semiconductor substrate and a channel is in the substrate under the gate (column 2, lines 42-45), further comprising forming a source/drain extension adjacent to the channel in the semiconductor substrate (309 in Fig. 3H).

Regarding claim 30, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches that forming comprises implanting a second source/drain dopant into the substrate for forming the source/drain extension, wherein the implanting the second source/drain dopant is performed prior to the implanting the boron (first boron implant region 305 becomes extension region 309; Figs. 3G-3H).

Regarding claim 31, Krishnan et al. and Koizumi et al. together teach the method of claim 1. Krishnan et al. further teaches activating the boron (column 3, lines 25-27).

Regarding claim 36, Krishnan et al. teaches a method of forming a semiconductor device, the method comprising:

- forming a gate (Fig. 3B) over a silicon substrate (301 in Fig. 3A), the substrate having a lattice having a lattice constant (Krishnan et al. teaches amorphizing and recrystallizing the substrate, so it inherently starts off as crystalline, and therefore has a lattice constant);
- increasing the lattice constant of the lattice in a source/drain region of the substrate after the forming the gate by implanting germanium at a dose between 1E13 and 1E17 atoms per centimeter squared using the gate as a mask (column 2 lines 60-66; column 3, lines 11-16 and lines 27-30; Krishnan et al. teaches recrystallizing the germanium-doped silicon substrate, which inherently creates a lattice having a larger lattice constant than silicon, since germanium is a larger atom);
- implanting boron into the source/drain region (column 2, line 66 – column 3, line 4; column 3, lines 18-21); and
- forming a nickel silicide over the portion of the source/drain region (column 3, lines 39-43).

Krishnan et al. does not teach that the implanting the boron is performed subsequent to the activating the germanium.

Koizumi et al. teaches a method of forming a transistor that comprises implanting germanium into a source/drain region, activating the germanium implant, and

subsequently doping the source/drain region. The method taught by Koizumi et al. ensures a good SiGe mixed crystal (column 11, lines 33-50).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Krishnan et al., and reverse the order of the germanium activation and dopant implant, as taught by Koizumi et al., since this method yields a good SiGe mixed crystal.

Regarding claim 44, Krishnan et al. teaches a method of forming a semiconductor device, the method comprising:

- forming a gate over a silicon semiconductor substrate (Fig. 3B);
- implanting particles including germanium into a region of the substrate after the forming the gate at a dose between 1E13 and 1E17 atoms per centimeter squared using the gate as a mask (column 2 lines 60-66; column 3, lines 11-16 and lines 27-30);
- activating the germanium implanted into the region (column 3, lines 27-32);
- implanting boron into the substrate for forming at least a portion of a source/drain region in the substrate (column 2, line 66 – column 3, line 4; column 3, lines 18-21); and
- forming a nickel silicide over the region after the activating ((column 3, lines 39-43).

Krishnan et al. does not teach that the implanting the boron is performed subsequent to the activating the germanium.

Koizumi et al. teaches a method of forming a transistor that comprises implanting germanium into a source/drain region, activating the germanium implant, and subsequently doping the source/drain region. The method taught by Koizumi et al. ensures a good SiGe mixed crystal (column 11, lines 33-50).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Krishnan et al., and reverse the order of the germanium activation and dopant implant, as taught by Koizumi et al., since this method yields a good SiGe mixed crystal.

Regarding claim 45, Krishnan et al. teaches in a transistor device structure having a gate stack (302B, 303B in Fig. 3B) and source/drain contact regions comprised primarily of a first material, wherein the source/drain contact regions have a lattice constant (Krishnan et al. teaches amorphizing and recrystallizing the substrate, so it inherently starts off as crystalline, and therefore has a lattice constant), a method of forming a contact, comprising:

- implanting germanium at a dose between 1E13 and 1E17 atoms per centimeter squared into the source/drain regions using the gate stack as a mask (column 2 lines 60-66; column 3, lines 11-16 and lines 27-30);
- activating the germanium implanted into the source/drain contact regions to increase the lattice constant of the source/drain contact regions (column 3, lines 27-30; Krishnan et al. teaches recrystallizing the germanium-doped silicon substrate, which inherently creates a lattice having a larger lattice constant than silicon, since germanium is a larger atom);

- implanting boron into the source/drain contact regions (column 2, line 66 – column 3, line 4; column 3, lines 18-21); and
- forming a nickel silicide over the source/drain contact regions after the step of activating.

Krishnan et al. does not teach that the implanting the boron is performed after the step of activating.

Koizumi et al. teaches a method of forming a transistor that comprises implanting germanium into a source/drain region, activating the germanium implant, and subsequently doping the source/drain region. The method taught by Koizumi et al. ensures a good SiGe mixed crystal (column 11, lines 33-50).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Krishnan et al., and reverse the order of the germanium activation and dopant implant, as taught by Koizumi et al., since this method yields a good SiGe mixed crystal.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. 6,399,452) in view of Koizumi et al. (U.S. 5,475,244), as applied to claim 1 above, and further in view of Downey (U.S. 2002/0187614).

Regarding claims 10 and 11, Krishnan et al. and Koizumi et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating further includes rapid thermal annealing or laser annealing of the source/drain contact regions.

Downey teaches a method of implanting silicon with germanium and activating the germanium by rapid thermal annealing and laser annealing (paragraph 0032).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Krishnan et al. and Koizumi et al. together and Downey by forming a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Krishnan et al. and Koizumi et al. together, by activating the germanium implant by rapid thermal annealing or laser annealing, as taught by Downey. The motivation for doing so at the time of the invention would have been to cause chemical bonding between the substrate and the implanted material, as taught by Downey (paragraph 0031).

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. 6,399,452) in view of Downey (U.S. 2002/0187614).

Regarding claims 34 and 35, Krishnan et al. teaches a method of forming a semiconductor device, the method comprising:

- providing a semiconductor substrate (301 in Fig. 3A);
- forming a gate over the semiconductor substrate (Fig. 3B);
- implanting germanium into a region of the semiconductor substrate at a dose between 1E13 and 1E17 atoms per centimeter squared using the gate as a mask (column 2 lines 60-66; column 3, lines 11-16 and lines 27-30);
- activating the germanium implanted into the region of the semiconductor substrate (column 3, lines 25-32); and

- forming a nickel silicide over the region after the activating (column 3, lines 39-43).

Krishnan et al. does not teach that the activation process is a non-activation process or that it includes one of arc lamp rapid thermal annealing or laser annealing of the region.

Downey teaches a method of implanting silicon with germanium and activating the germanium by rapid thermal annealing and laser annealing, non-diffusion activation processes (paragraph 0032).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Krishnan et al. and Downey by forming a contact to a source/drain contact region of a transistor device, as taught by Krishnan et al., by activating the germanium implant by rapid thermal annealing or laser annealing, as taught by Downey. The motivation for doing so at the time of the invention would have been to cause chemical bonding between the substrate and the implanted material, as taught by Downey (paragraph 0031).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. 6,399,452) in view of Koizumi et al. (U.S. 5,475,244), as applied to claim 1 above, in view of Imai (U.S. 5,506,427).

Regarding claim 12, Krishnan et al. and Koizumi et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating further includes arc lamp thermal annealing of the source/drain contact region.

Imai teaches a method of annealing SiGe by arc lamp annealing (column 6, lines 7-10).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Krishnan et al. and Koizumi et al. together and Imai by forming a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Krishnan et al. and Koizumi et al. together, by activating the germanium implant by laser arc annealing, as taught by Imai. The motivation for doing so at the time of the invention would have been to avoid degrading transistor characteristics, as expressly taught by Imai (column 5, line 66 – column 6, line 2).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. 6,399,452) in view of Koizumi et al. (U.S. 5,475,244), as applied to claim 1 above, and further in view of Murakoshi et al. (U.S. 5,770,512).

Regarding claim 13, Krishnan et al. and Koizumi et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating includes gas convection annealing of the source/drain contact region.

Murakoshi et al. teaches a method of activating germanium ion-implanted into silicon by convectively heating it in a nitrogen gas atmosphere at 550°C for an hour to recrystallize the silicon wafer following ion implantation (column 14, lines 44-52).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region according to the method of claim 1 as taught by Krishnan et al. and Koizumi et al. together, and use

gas convection annealing to activate the germanium implantation, as taught by Murakoshi et al. The motivation for doing so at the time of the invention would have been to recrystallize the silicon wafer following ion implantation, as noted above and taught by Murakoshi et al.

Claims 14 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. 6,399,452) in view of Koizumi et al. (U.S. 5,475,244), as applied to claims 1 and 19 above, and further in view of Erokhin et al. (U.S. 2003/0087504).

Regarding claims 14 and 25, Krishnan et al. and Koizumi et al. together teach the method of claims 1 and 19 (note 35 U.S.C. 103(a) rejection above), but do not teach implanting the germanium at a temperature between 25 and 600 °C.

Erokhin et al. teaches a method of implanting germanium into silicon at a temperature between 25 and 600 °C (paragraphs 0011-0012).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Krishnan et al. and Koizumi et al. together and Erokhin et al. by forming contact to a source/drain region of a transistor using the method of claim 1, as taught by Krishnan et al. and Koizumi et al. together, by implanting germanium at a temperature between 25 and 600 °C, as taught by Erokhin et al., since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233 (CCPA 1955)).

Allowable Subject Matter

Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest, in combination with the other claimed limitations, activating the germanium by heating the source/drain region to a temperature of greater than 1000 °C or in a range of approximately 900 – 1400 °C. Although it is known in the art of semiconductor processing to use these high temperatures to activate germanium implants in silicon, Krishnan et al. expressly teaches using a low-temperature activation process at a temperature of 600 °C to avoid activating dopants in regions outside of the germanium-implanted regions. It would therefore render the invention taught by Krishnan et al. inoperable to combine this reference with other relevant references to arrive at the invention as recited in claims 8 and 9.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 7, 10-14, 17-22, 25, 26, 28, 30, 31, 34-36, 44, and 45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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